LED PCB Design Checklist

Complete Verification Guide for Professional LED Circuit Board Design

Version: 2.0
Date: January 2026
Purpose: Systematic verification checklist ensuring LED PCB designs meet thermal, electrical, and manufacturing requirements

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Section 1: Project Initialization

1.1 Requirements Definition

- **LED specifications documented**
    - Part number, manufacturer
    - Forward voltage (Vf) min/typ/max
    - Forward current (If) rated and maximum
    - Power rating per LED
    - Thermal resistance (Rth j-c)
    - Color temperature / wavelength
    - Beam angle specifications
- **Total power calculation completed**
    - Individual LED power: ___W each
    - Total LED count: ___
    - Total electrical power: ___W
    - Total thermal power: ___W (60-70% of electrical)
    - Power density: ___W/cm²
- **Operating environment defined**
    - Ambient temperature range: ___ to ___°C
    - Humidity conditions

- Vibration/shock requirements
- Indoor/outdoor classification
- Enclosure type (sealed, ventilated, open)

- **Target specifications established**
  - Target junction temperature: <___°C (recommend <75-85°C)
  - Expected lifespan: ___hours
  - Warranty period: ___years
  - Budget constraints per board: $___

Section 2: Thermal Design Calculations

2.1 Junction Temperature Prediction

- **Heat dissipation calculated for each LED**
  - Formula verified: P_thermal = P_electrical × (1 - Efficiency)
  - LED efficiency assumed: ___%
  - Safety margin included (15-20%)
  - Individual LED thermal power: ___W
- **Thermal resistance chain calculated**
  - Rth_j-c (LED datasheet): ___°C/W
  - Rth_c-pcb (solder joint): ~1-3°C/W
  - Rth_pcb (through dielectric): ___°C/W
  - Rth_interface (TIM): ___°C/W
  - Rth_heatsink (if applicable): ___°C/W
  - **Total Rth**: ___°C/W
- **Junction temperature estimated**
  - Formula: Tj = T_ambient + (P_thermal × Rth_total)
  - Worst-case ambient: ___°C
  - Calculated Tj: ___°C

- Verification: Tj < Target temperature? **YES / NO**
- If NO: Redesign substrate or add cooling

2.2 Power Density Analysis

- **PCB area determined**: ___cm²
- **Power density calculated**: ___W/cm²
- **Substrate selection guideline checked**:
  - <0.5 W/cm²: Aluminum adequate
  - 0.5-1.5 W/cm²: Aluminum recommended
  - 1.5-3 W/cm²: Copper or enhanced cooling
  - 3 W/cm²: Ceramic or active cooling

Section 3: Substrate Selection

3.1 Material Selection

- **Substrate type selected**:
  - FR4 (only for <0.5W per LED)
  - Aluminum MCPCB (most common)
  - Copper core MCPCB (high power)
  - Aluminum oxide ceramic (premium)
  - Aluminum nitride ceramic (ultimate)
  - Flexible (low power only)
  - Hybrid (specify zones)
- **Substrate specifications documented**
  - Base material: ___
  - Base thickness: ___mm
  - Thermal conductivity (through dielectric): ___W/mK
  - Dielectric thickness: ___μm
  - Dielectric breakdown voltage: ___V

- **Selection rationale documented**
    - Thermal requirements met
    - Cost within budget
    - Availability confirmed
    - Lead time acceptable

3.2 Copper Specification

- **Copper weight selected**:
    - 1oz (35µm) - only if low power
    - **2oz (70µm) - RECOMMENDED for most LED applications**
    - 3oz (105µm) - high power applications
- **Justification documented**:
    - Thermal spreading requirements
    - Current carrying capacity
    - Cost-benefit analysis

Section 4: Thermal Management Design

4.1 Copper Distribution

- **Copper pour maximized**
    - All unused area filled with copper (solid fills)
    - No hatched/meshed fills in thermal zones
    - Continuous copper planes (no unnecessary breaks)
    - Copper extends to board edges where practical
- **LED thermal zones designed**
    - Solid copper under each LED (minimum)
    - Copper extends 15-30mm beyond LED in all directions
    - Thermal pathways to heat sink/mounting points
    - No narrow bottlenecks in thermal paths

4.2 Thermal Via Design

- **Via quantity calculated per LED**
    - LED power: ___W
    - Target via count: ___ (guideline: 1.5-2.5 vias per watt)
    - Actual via count: ___
    - Verification: Adequate? **YES / NO**
- **Via specifications defined**
    - Via drill diameter: ___mm (typical 0.3-0.5mm)
    - Via pad diameter: ___mm
    - Via spacing: ___mm (typical 1.0-1.5mm)
    - Pattern: [ ] Grid [ ] Staggered
- **Via placement designed**
    - Vias cover entire LED thermal pad area
    - Vias extend slightly beyond pad edges
    - Center area allows solder flow (avoid via in exact center)
    - Via arrays positioned for optimal thermal transfer
- **Via treatment specified**
    - Open (standard, lowest cost)
    - Tented (solder mask covered)
    - Plugged (non-conductive epoxy)
    - Filled (conductive epoxy, best thermal)

4.3 LED Placement and Spacing

- **LED spacing verified**
    - Minimum spacing met for LED power level:
        - <1W: 15-20mm center-to-center
        - 1-3W: 30-40mm center-to-center
        - 3-5W: 45-60mm center-to-center

        - 5W: 60mm+ center-to-center
    - Edge clearance: ___mm (minimum 15mm recommended)
- **Thermal interaction evaluated**
    - Thermal zone overlap minimal
    - Hot spots identified and mitigated
    - Symmetrical layout for uniform temperature
- **Optical requirements satisfied**
    - Light distribution uniform
    - Beam overlap appropriate
    - Color mixing adequate (RGB applications)

4.4 Heat Sink Integration

- **Heat sink requirements determined**
    - Heat sink needed? **YES / NO**
    - If YES:
        - Required thermal resistance: ___°C/W
        - Heat sink type: ___
        - Attachment method: [ ] Screws [ ] Clips [ ] Adhesive
- **Thermal interface specified**
    - TIM type: [ ] Grease [ ] Pad [ ] Phase-change [ ] Adhesive
    - Thermal conductivity: ___W/mK
    - Thickness: ___mm
    - Application method: ___
- **Mounting design completed**
    - Mounting hole locations defined
    - Clamping pressure adequate (2-5 psi)
    - Contact area maximized
    - Surface flatness specified (<0.1mm)

Section 5: Electrical Design

5.1 LED Circuit Topology

- **Topology selected**:
    - Series strings
    - Parallel arrays
    - Series-parallel combination
    - Rationale documented
- **String calculations completed**
    - LEDs per string: ___
    - Number of strings: ___
    - String voltage (min/typ/max): ___ / ___ / ___V
    - Current per string: ___mA
    - Total current: ___A
- **Current balancing method defined**
    - Series (inherent balancing)
    - Resistors per LED/string
    - Active current regulators
    - Separate drivers per string

5.2 LED Driver Selection

- **Driver specifications**
    - Part number: ___
    - Output current: ___mA (matches LED requirements)
    - Output voltage range: ___ to ___V (accommodates string voltage)
    - Efficiency: ___% (>85% recommended)
    - Dimming support: [ ] PWM [ ] Analog [ ] None
- **Protection features verified**

    - Over-voltage protection: **YES / NO**
    - Over-current protection: **YES / NO**
    - Thermal shutdown: **YES / NO**
    - Short-circuit protection: **YES / NO**
- **Driver placement planned**
    - Location: ___ (away from high-power LEDs preferred)
    - Thermal management: ___
    - EMI considerations: ___

5.3 Trace Width Calculations

- **Power trace widths calculated**
    - LED string current: ___A
    - Trace length: ___mm
    - Copper weight: ___oz
    - Calculated minimum width: ___mm
    - Design width (with margin): ___mm
    - Verification: IPC-2152 compliant? **YES / NO**
- **Voltage drop verified**
    - Calculated voltage drop: ___mV
    - Percentage of LED voltage: ___%
    - Acceptable (<2% target)? **YES / NO**
- **Ground return paths adequate**
    - Ground trace widths match power traces
    - Ground plane used where possible
    - Multiple ground return paths provided

5.4 Protection Circuits

- **Over-current protection implemented**
    - Driver built-in current limit

- Fuse (rating: ___mA/A)
- Resettable fuse (PPTC)
- Active current limiting circuit

- **ESD protection added**
  - TVS diodes at power input (breakdown voltage: ___V)
  - TVS diodes at control inputs
  - Series resistors for current limiting
  - ESD rating target: ___kV (IEC 61000-4-2)

Section 6: PCB Layout

6.1 Component Placement

- **LED positions optimized**
  - Thermal requirements met
  - Optical requirements met
  - Spacing verified
  - Orientation consistent and marked
- **Driver IC placement optimized**
  - Thermal isolation from LEDs
  - Support components nearby (<10-15mm)
  - EMI considerations addressed
  - Thermal relief provided
- **Passive components placed**
  - Decoupling caps close to pins (<5-10mm)
  - Bulk caps near driver output (<25mm)
  - Current sense resistors properly located
  - Component values labeled (optional)
- **Connectors positioned**

    - Accessible locations
    - Mechanical support adequate
    - Clearance for mating/cable bending
    - Polarity clearly marked

6.2 Routing

- **Power trace routing completed**
    - Adequate width (per calculations)
    - Direct paths (minimal length)
    - No unnecessary narrow sections
    - Solid copper pours integrated
- **Signal routing completed**
    - Control signals routed away from switching nodes
    - PWM traces short and direct
    - Ground reference provided
    - Cross-talk minimized
- **Ground design implemented**
    - Ground plane on bottom layer (or designated layer)
    - Ground plane continuous (no breaks)
    - Via stitching every 20-40mm
    - All grounds connect to plane

6.3 EMI/EMC Considerations

- **Layout optimized for low EMI**
    - Switching node loop area minimized
    - Driver components tightly grouped
    - Input/output filtering added
    - Ground plane provides shielding
- **External connections protected**

- Ferrite beads on cables (if needed)
- ESD protection at connectors
- Twisted pair for LED outputs (optional)

Section 7: Design Rules and Manufacturing

7.1 Design Rule Compliance

- **Trace width and spacing**
  - Minimum trace width: ___mm (verify manufacturable)
  - Minimum spacing: ___mm (voltage-appropriate)
  - Power trace widths per calculations
  - Design rule check (DRC) passed: **YES / NO**
- **Via specifications**
  - Drill size: ___mm
  - Pad diameter: ___mm
  - Annular ring: ___mm (>0.10mm minimum)
  - Clearances adequate
- **Solder mask specifications**
  - Minimum dam between pads: ___mm (>0.10mm)
  - Solder mask expansion: ___mm per side (typically 0.10mm)
  - Vias tented where required
  - Color: ___ (green standard)
- **Silkscreen specifications**
  - Text height: ___mm (>1.0mm minimum, 1.5mm recommended)
  - Line width: ___mm (>0.15mm minimum, 0.20mm recommended)
  - Component designators clear
  - Polarity marks present
  - Version/revision marked

7.2 Design for Manufacturing (DFM)

- **Manufacturer capabilities verified**
    - Minimum feature sizes within capabilities
    - Copper weight available
    - Substrate type offered
    - Lead time acceptable
- **Manufacturing notes prepared**
    - Substrate specification clear
    - Copper weight specified
    - Surface finish specified (HASL, ENIG, OSP)
    - Via treatment specified
    - Special instructions documented
- **Panelization considered**
- Production quantities determine panelization
- Tooling holes/fiducials included
- Breakaway tabs/v-score specified
- Panel size optimized for cost
- **7.3 Assembly Considerations**
- **Component package selection**
- Standard packages used where possible
- Pick-and-place compatible
- Hand assembly feasible (if low volume)
- Thermal pad design appropriate
- **Assembly documentation prepared**
- Bill of Materials (BOM) complete
- Assembly drawing created
- Pick-and-place file generated

- Component placement list provided
- **Solder paste considerations**
- Stencil aperture design appropriate
- Thermal vias don't cause solder wicking (tented/plugged)
- Adequate solder volume for thermal pads
- Reflow profile compatible with all components
- **Test point access**
- Test points at key nodes (power, LED strings, control signals)
- 0.1" spacing for probe clips
- Accessible from top side
- Clearly labeled
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- **Section 8: Thermal Simulation (Recommended for >10W designs)**
- **8.1 Simulation Setup**
- **Thermal model created**
- Software used: ___
- PCB geometry modeled accurately
- Material properties entered (substrate, copper, LEDs)
- Boundary conditions defined (ambient temp, convection)
- **Heat sources defined**
- LED power dissipation per component: ___W
- Driver heat dissipation: ___W
- Total heat load: ___W
- Heat distribution verified
- **Cooling conditions modeled**
- Natural convection: ___W/m²·K
- Forced air (if applicable): ___m/s, ___CFM

- Heat sink modeled (if present)
- Thermal interface properties included
- **8.2 Simulation Results**
- **Temperature distribution analyzed**
- Maximum LED junction temperature: ___°C
- Target junction temperature: ___°C
- Verification: Within limits? **YES / NO**
- Hot spots identified: ___
- **Thermal pathways verified**
- Heat flow paths visualized
- Bottlenecks identified
- Thermal via effectiveness confirmed
- Heat spreading adequate
- **Design optimization (if needed)**
- Increased copper thickness: **YES / NO**
- Added thermal vias: **YES / NO**
- Changed LED spacing: **YES / NO**
- Upgraded substrate: **YES / NO**
- Added heat sink: **YES / NO**
- **8.3 Worst-Case Analysis**
- **Maximum ambient temperature simulated**: ___°C
- **Maximum power condition verified**
- **Thermal margin calculated**: ___°C below Tj_max
- **Safety margin adequate (>10-15°C)**: **YES / NO**
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- **Section 9: Pre-Fabrication Review**
- **9.1 Design Files Check**

- **Gerber files generated**
- Top copper layer
- Bottom copper layer (if applicable)
- Top solder mask
- Bottom solder mask
- Top silkscreen
- Bottom silkscreen (if applicable)
- Drill file
- Board outline
- **File verification**
- Gerber viewer check performed
- All layers aligned correctly
- No missing features
- Drill hits match pads
- **Manufacturing documentation**
- Fabrication drawing created
- Layer stack-up documented
- Material specifications clear
- Special instructions included
- Revision number/date marked
- **9.2 Design Review Checklist**
- **Electrical review**
- Schematic matches layout
- Net connections verified
- Polarity correct on all components
- Power supply voltages correct
- No floating nets

- **Thermal review**
- All thermal calculations documented
- Thermal vias under all LEDs
- Copper pours maximized
- Heat sink interface designed
- **Mechanical review**
- Board dimensions correct
- Mounting holes positioned correctly
- Connector heights verified
- Enclosure fit confirmed
- Weight acceptable
- **Manufacturing review**
- DFM check passed
- All design rules met
- Standard components used
- Assembly complexity acceptable
- Cost estimate within budget
- **9.3 Peer Review**
- **Design reviewed by colleague/expert**
- Reviewer name: ___
- Review date: ___
- Issues identified: ___
- Issues resolved: **YES / NO**
- **Critical items verified**
- LED polarity correct
- Power connections correct
- Driver configuration verified

- Thermal design adequate
- Safety/regulatory compliance
- ---
- **Section 10: Prototype Phase**
- **10.1 Prototype Order**
- **Manufacturer selected**
- Company: ___
- Contact: ___
- Quote received: $___
- Lead time: ___days
- Minimum order quantity: ___
- **Order specifications**
- Quantity: ___ boards
- Substrate: ___
- Copper weight: ___oz
- Surface finish: ___
- Solder mask color: ___
- Silkscreen color: ___
- Via treatment: ___
- Special requirements: ___
- **Assembly planning**
- In-house assembly
- Contract assembly
- Components ordered: **YES / NO**
- Assembly timeline: ___
- **10.2 Prototype Inspection (Upon Receipt)**
- **Visual inspection**

- Board dimensions correct
- No visible damage
- Solder mask quality good
- Silkscreen legible
- Copper finish acceptable
- **Electrical inspection**
- Continuity test passed
- No shorts between nets
- Via plating intact
- Pad adhesion good
- **Thermal inspection**
- Thermal vias present and plated
- Copper pours intact
- Metal base flat (if MCPCB)
- Thermal pad quality good
- **10.3 Assembly Testing**
- **Components assembled**
- LEDs mounted correctly (polarity verified)
- Driver IC soldered properly
- Passive components in place
- Connectors attached securely
- **Assembly quality check**
- No solder bridges
- No cold solder joints
- Component alignment good
- No missing components
- ---

- **Section 11: Functional Testing**
- **11.1 Initial Power-Up**
- **Pre-power checks**
- Visual inspection passed
- Polarity verified
- No obvious shorts
- Correct input voltage source ready
- **First power-up**
- Input voltage: ___V (start at low voltage/current limit)
- Current consumption: ___mA (verify reasonable)
- No smoke/smell/overheating
- LEDs illuminate: **YES / NO**
- **Basic functionality**
- All LEDs light up
- Brightness uniform
- Color correct
- Dimming works (if applicable)
- **11.2 Electrical Measurements**
- **Voltage measurements**
- Input voltage: ___V (verify correct)
- LED string voltage: ___V (within expected range?)
- Driver output voltage: ___V
- Any unexpected voltages: ___
- **Current measurements**
- Total input current: ___mA
- LED string current: ___mA (matches design?)
- Driver current consumption: ___mA

- Efficiency: ___%
- **LED forward voltage**
- Measure individual LED Vf: ___ to ___V
- Within datasheet range: **YES / NO**
- String voltage sum correct: **YES / NO**
- **11.3 Thermal Testing**
- **Critical for LED PCB validation!**
- **Temperature measurement setup**
- Method: [ ] Thermal camera [ ] Thermocouple [ ] IR thermometer
- Ambient temperature: ___°C
- Stabilization time: ___ minutes (30+ minutes recommended)
- Operating at full power: **YES / NO**
- **LED junction temperature measurement**
- Method used: [ ] Thermal camera [ ] Vf method [ ] Datasheet calculation
- Maximum Tj measured: ___°C
- Target Tj: ___°C
- Verification: Tj < Target? **YES / NO**
- Thermal margin: ___°C
- **PCB temperature distribution**
- Hottest spot location: ___
- Hottest spot temperature: ___°C
- Temperature uniformity: Good / Acceptable / Poor
- Hot spots identified: ___
- **Driver IC temperature**
- Driver case temperature: ___°C
- Maximum allowed: ___°C (datasheet)
- Adequate cooling: **YES / NO**

- **Thermal performance verification**
- Measured vs. predicted temperatures:
- Predicted Tj: ___°C
- Measured Tj: ___°C
- Difference: ___°C (should be within ±10-15°C)
- Thermal design adequate: **YES / NO**
- **11.4 Long-Term Stability Testing**
- **Burn-in test**
- Duration: ___hours (24-48 hours recommended)
- Operating conditions: Full power, elevated ambient
- Temperature monitoring: Continuous / Periodic
- No failures observed: **YES / NO**
- **Thermal cycling test (optional but recommended)**
- Number of cycles: ___
- Temperature range: ___ to ___°C
- No solder joint failures: **YES / NO**
- No LED performance degradation: **YES / NO**
- **11.5 EMI/EMC Testing (If Required)**
- **Pre-compliance testing**
- Conducted emissions measured
- Radiated emissions measured
- Results within limits: **YES / NO**
- Mitigation needed: ___
- **ESD testing**
- Contact discharge: ___kV (target ⩾4kV)
- Air discharge: ___kV (target ⩾8kV)
- Protection adequate: **YES / NO**

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- **Section 12: Design Validation**
- **12.1 Performance Verification**
- **Specifications met**
- Light output: ___lumens (target: ___)
- Efficiency: ___% (target: ___)
- Power consumption: ___W (target: ___)
- Color temperature: ___K (target: ___)
- All specifications within tolerance: **YES / NO**
- **Thermal performance validated**
- Junction temperature: ***°C (target: <***°C) ✓
- Thermal margin adequate: **YES / NO**
- Expected lifespan: ___hours (based on Tj)
- Meets requirement: **YES / NO**
- **Reliability assessment**
- No failures during testing: **YES / NO**
- Thermal stress acceptable
- Electrical stress acceptable
- Mechanical integrity good
- **12.2 Issues and Resolutions**
- **Issues identified during testing**:
- Issue: ___
- Severity: [ ] Critical [ ] Major [ ] Minor
- Resolution: ___
- Status: [ ] Resolved [ ] Pending [ ] Deferred
- Issue: ___

- Severity: [ ] Critical [ ] Major [ ] Minor
- Resolution: ___
- Status: [ ] Resolved [ ] Pending [ ] Deferred
- Issue: ___
- Severity: [ ] Critical [ ] Major [ ] Minor
- Resolution: ___
- Status: [ ] Resolved [ ] Pending [ ] Deferred
- **All critical issues resolved**: **YES / NO**
- **Design revision needed**: **YES / NO**
- If YES: Revision number: ___
- **12.3 Production Readiness**
- **Prototype validation complete**
- All tests passed
- Performance meets requirements
- Reliability demonstrated
- Ready for production: **YES / NO**
- **Manufacturing documentation finalized**
- Production Gerbers approved
- BOM finalized
- Assembly instructions complete
- Test procedures documented
- Quality acceptance criteria defined
- **Cost and timeline confirmed**
- Production unit cost: $___
- Lead time: ___weeks
- MOQ: ___units
- Within project budget: **YES / NO**

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- **Section 13: Final Sign-Off**
- **13.1 Design Approval**
- **Design Engineer:** _____ Date: _____
- **Thermal Engineer:** _____ Date: _____
  (If applicable)
- **Project Manager:** _____ Date: _____
- **Quality Engineer:** _____ Date: _____
- **13.2 Ready for Production**
- All checklist items completed
- All tests passed
- All approvals obtained
- Manufacturing documentation ready
- **APPROVED FOR PRODUCTION**
- **Appendix A: Quick Reference Tables**
- **LED PCB Substrate Selection Guide**

Power Density	Ambient Temp	Recommended Substrate
<0.5 W/cm²	<30°C	Aluminum MCPCB
0.5-1.5 W/cm²	<50°C	Aluminum MCPCB (2oz copper)
1.5-3 W/cm²	<50°C	Copper core or forced cooling
>3 W/cm²	Any	Ceramic or active cooling
Any	>70°C	Ceramic substrate

- **Thermal Via Guidelines**

LED Power	Recommended Via Count	Via Pattern
<0.5W	2-4 vias	Simple array

- **LED Power**
- **Recommended Via Count**
- **Via Pattern**
- 0.5-1W
- 4-6 vias
- Grid under pad
- 1-3W
- 6-12 vias
- Dense grid
- 3-5W
- 12-20 vias
- Full coverage
- >5W
- 20+ vias
- Maximum density

- **Trace Width Reference (2oz Copper, 10°C Rise)**

- **Current**
- **Minimum Width**
- **Recommended Width**
- 350mA
- 0.5mm
- 1.0mm
- 700mA
- 1.0mm
- 1.5mm
- 1A
- 1.5mm
- 2.5mm
- 2A
- 2.5mm
- 4.0mm
- 3A+
- Use power plane
- 5mm+ trace

- **LED Spacing Guidelines**

- **LED Power**
- **Minimum Center-to-Center**
- <0.5W
- 15-20mm
- 0.5-1W
- 20-30mm
- 1-3W
- 30-40mm
- 3-5W
- 45-60mm
- >5W
- 60mm+

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- **Appendix B: Common Issues and Solutions**
- **Problem: LEDs Overheat (Tj > Target)**
- **Possible Causes:**
- Insufficient thermal vias
- Inadequate copper pour

- Poor LED spacing
- Wrong substrate selection
- Inadequate heat sink
- **Solutions:**
- Add more thermal vias (double the count)
- Increase copper thickness to 3oz
- Increase LED spacing by 30-50%
- Upgrade to copper core substrate
- Add external heat sink with TIM
- Reduce LED drive current by 20-30%
- **Problem: Uneven LED Brightness**
- **Possible Causes:**
- Parallel LED connection without current balancing
- Vf mismatch between LEDs
- Poor current regulation
- Thermal variation causing Vf shift
- **Solutions:**
- Use series string topology
- Add current balancing resistors
- Purchase LEDs from same manufacturing bin
- Improve thermal uniformity
- Use separate constant-current drivers per string
- **Problem: High Voltage Drop in Traces**
- **Possible Causes:**
- Traces too narrow
- Traces too long
- Inadequate copper weight

- Poor connections/vias
- **Solutions:**
- Widen power traces (double width reduces drop by 50%)
- Shorten trace routing paths
- Upgrade to 2oz or 3oz copper
- Use power planes instead of traces
- Add parallel traces for high current paths
- **Problem: LED Flicker During Dimming**
- **Possible Causes:**
- PWM frequency too low (<500Hz)
- Capacitance on LED causing exponential decay
- Driver PWM response too slow
- Noise on PWM signal
- **Solutions:**
- Increase PWM frequency to 2-5kHz minimum
- Remove/reduce output capacitance
- Select driver with fast PWM response specs
- Filter PWM control signal (100Ω + 100nF)
- Use analog dimming instead of PWM
- **Problem: EMI/EMC Compliance Failure**
- **Possible Causes:**
- Large switching node loop area
- No input/output filtering
- Long LED cable without ferrite
- No ground plane
- Driver components too spread out
- **Solutions:**

- Minimize switching node loop area
- Add common-mode choke at input
- Add output capacitors close to LEDs
- Implement solid ground plane
- Add ferrite beads on cables
- Group switching components tightly
- Use metal enclosure grounded to PCB
- **Problem: Solder Wicking into Thermal Vias**
- **Possible Causes:**
- Vias not tented/plugged
- Too much solder paste
- Vias too large
- **Solutions:**
- Specify tented vias (solder mask over)
- Plug vias with epoxy
- Reduce solder paste volume (smaller aperture)
- Use smaller via diameter (0.3mm instead of 0.5mm)
- **Problem: Poor Thermal Contact to Heat Sink**
- **Possible Causes:**
- Air gaps between PCB and heat sink
- Inadequate clamping pressure
- Poor thermal interface material
- Warped PCB or heat sink
- **Solutions:**
- Use compliant thermal pad to fill gaps
- Increase number of mounting screws
- Torque screws to specification (0.5-1.5 N·m)

- Specify flatness tolerance (<0.1mm)
- Use phase-change TIM
- Add more mounting points for large boards
- ---
- **Appendix C: Useful Formulas**
- **Thermal Calculations**
- **LED Thermal Power Dissipation:**
- P_thermal = P_electrical × (1 - Efficiency)
- P_thermal = Vf × If × (1 - η)
- **Junction Temperature:**
- Tj = T_ambient + (P_thermal × Rth_total)
- Rth_total = Rth_j-c + Rth_c-pcb + Rth_pcb + Rth_interface + Rth_sink
- **Thermal Resistance:**
- Rth = ΔT / P
- ΔT = Temperature rise (°C)
- P = Power dissipated (W)
- **Electrical Calculations**
- **Resistor Current Limiting:**
- R = (Vsupply - LED_Vf) / LED_If
- P_resistor = (Vsupply - Vf) × If
- **Trace Resistance:**
- R_trace (mΩ) = 0.5 × L(mm) / [W(mm) × T(oz)]
- L = length, W = width, T = copper thickness
- **Voltage Drop:**
- V_drop = I × R_trace
- V_drop = I × (ρ × L / A)
- ρ = copper resistivity (1.72×10^{-8} Ω·m)

- **Power Density:**
- Power_Density (W/cm²) = Total_Power (W) / PCB_Area (cm²)
- **LED String Calculations**
- **Maximum LEDs in Series:**
- Max_LEDs = (Driver_Vmax - Headroom) / LED_Vf_typical
- **String Voltage Range:**
- V_string_min = LEDs_per_string × LED_Vf_min
- V_string_max = LEDs_per_string × LED_Vf_max
- **Total Current (Parallel Strings):**
- I_total = Number_of_strings × I_per_string
- ---
- **Appendix D: Online Tools and Resources**
- **Trace Width Calculators**
- **CircuitCalculator.com** - PCB Trace Width Calculator (IPC-2152)
- **Saturn PCB Toolkit** - Professional calculator suite (free download)
- **DigiKey Calculator** - Integrated with component search
- **4PCB Calculator** - Simple web-based tool
- **Thermal Simulation Software**
- **ANSYS Icepak** - Professional FEA thermal simulation
- **FloTHERM** - Electronics cooling simulation
- **SolidWorks Flow Simulation** - Integrated with CAD
- **SimScale** - Cloud-based thermal simulation (free tier available)
- **PCB Design Software**
- **Altium Designer** - Industry standard (commercial)
- **KiCad** - Open source, fully featured (free)
- **Eagle/Fusion 360** - User-friendly (Autodesk)
- **EasyEDA** - Web-based, free option

- **LED Datasheet Resources**
- **Cree LED** - www.cree.com
- **Lumileds** - www.lumileds.com
- **Nichia** - www.nichia.com
- **Osram Opto Semiconductors** - www.osram.com
- **Samsung LED** - www.samsung.com/led
- **Standards and References**
- **IPC-2152** - Current Carrying Capacity Standards
- **IPC-6012** - Rigid PCB Qualification Standard
- **IPC-7095** - Design and Assembly Process for BGAs
- **IEC 61000-4-2** - ESD Immunity Testing
- **CISPR 15** - EMC Requirements for Lighting Equipment
- ---
- **Appendix E: Glossary of Terms**
- **MCPCB** - Metal Core Printed Circuit Board, LED PCB with aluminum/copper base
- **Tj** - Junction Temperature, operating temperature of LED semiconductor die
- **Vf** - Forward Voltage, voltage drop across LED when conducting
- **If** - Forward Current, current through LED for specified brightness
- **Rth** - Thermal Resistance, resistance to heat flow (°C/W)
- **TIM** - Thermal Interface Material, improves heat transfer between surfaces
- **CTE** - Coefficient of Thermal Expansion, material expansion per degree
- **DRC** - Design Rule Check, automated verification of design rules
- **DFM** - Design for Manufacturing, design practices for manufacturability
- **PWM** - Pulse Width Modulation, dimming method using on/off switching
- **TVS** - Transient Voltage Suppressor, ESD protection device
- **ESD** - Electrostatic Discharge, sudden voltage/current from static electricity

- **EMI** - Electromagnetic Interference, unwanted electromagnetic radiation
- **EMC** - Electromagnetic Compatibility, ability to operate without EMI issues
- **AOI** - Automated Optical Inspection, machine vision quality control
- **SMT** - Surface Mount Technology, components mounted on PCB surface
- **HASL** - Hot Air Solder Leveling, PCB surface finish method
- **ENIG** - Electroless Nickel Immersion Gold, premium surface finish
- **Via Tenting** - Covering via with solder mask to prevent solder wicking
- **Via Plugging** - Filling via with epoxy to prevent solder wicking
- **Thermal Via** - Via designed primarily for heat conduction, not electrical connection
- **Ground Plane** - Large continuous copper area connected to ground
- **Copper Pour** - Filling unused PCB area with copper
- **Annular Ring** - Copper ring around drilled hole (pad to hole clearance)
- **Solder Mask Dam** - Solder mask between adjacent pads preventing bridges
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- **Document Revision History**

Version	Date	Changes	Author
1.0	Jan 2025	Initial release	LED Engineering Team
2.0	Jan 2026	Added thermal simulation section, expanded testing checklist	LED Engineering Team

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- **Notes and Project-Specific Information**
- **Project Name:** _____
- **Designer:** _____

- **Date Started:** _____
- **Target Completion:** _____
- **Special Requirements:**
- _____
- _____
- _____
- **Lessons Learned:**
- _____
- _____
- _____
- **Follow-Up Actions:**
- _____
- _____
- _____
- _____
- **Contact Information for Support**
- **For design consultation, thermal analysis, or manufacturing services:**
- **Website:** Https://www.pcbelec.com
- **Technical Support:** engineer@pcbjhy.com
- **LED PCB Manufacturing Service:** sales@pcbjhy.com
- **Design Services:** Free initial consultation, thermal simulation, DFM review
- **Manufacturing:** Aluminum, copper, ceramic LED PCBs | Prototyping and production
- **Quality:** ISO 9001:2015 certified | UL recognized | RoHS compliant

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END OF LED PCB DESIGN CHECKLIST